IN THE ABSTRACT:

Please replace the abstract with the following amended paragraph showing changes. A clean copy of the amended abstract is on the following page.

ABSTRACT OF THE DISCLOSURE

For use in a wide-issue pipelined processor, a mechanism for, and method of, reducing pipeline stalls between conditional branches and a digital signal processor (DSP) incorporating the mechanism or the method. In one embodiment, the mechanism includes: (1) a mispredict program counter (PC) generator that generates a mispredict PC value for each conditional branch instruction in a pipeline of the processor and (2) mispredict PC storage, coupled to the mispredict PC generator, that stores the mispredict PC value at least until a resolution of the conditional branch instruction occurs and makes the mispredict PC value available to a PC of the processor if the resolution results in a mispredict condition. The mispredict PC storage includes a mispredict PC queue and a number of staging registers wherein the mispredict PC queue has at least as many stages as the number of staging registers.

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For use in a wide-issue pipelined processor, a mechanism for, and method of, reducing pipeline stalls between conditional branches and a digital signal processor (DSP) incorporating the mechanism or the method. In one embodiment, the mechanism includes: (1) a mispredict program counter (PC) generator that generates a mispredict PC value for each conditional branch instruction in a pipeline of the processor and (2) mispredict PC storage, coupled to the mispredict PC generator, that stores the mispredict PC value at least until a resolution of the conditional branch instruction occurs and makes the mispredict PC value available to a PC of the processor if the resolution results in a mispredict condition. The mispredict PC storage includes a mispredict PC queue and a number of staging registers wherein the mispredict PC queue has at least as many stages as the number of staging registers.